AMENDMENT RESPONSIVE TO OFFICE ACTION

IN THE SPECIFICATIION

Applicant amends the Specification as follows:

On page 6 line 6 change "integrated" to "integrator".

On page 6 line 8 change "quantifier" to "quantizer".

Marked Up Paragraph:

Referring to Figures 1A and 1B, first and second order modulators have been to modulate an analog input signal 10 into a modulated output 12. The output 12 is a binary output. In the first order sigma delta modulator of Figure 1 A. The input signal in fed into a summer 14 providing an input error signal that is fed into an ~~integrated~~ integrator 16. The input error signal from the summer 14 is integrated by the integrator 16 to form an accumulated error signal that becomes an input to a one bit ~~quantifier~~ quantizer 18. The output of the one bit quantizer 18 is the binary output 12 and is the sign of accumulated error signal. The output of the quantizer 18 is fed into the DAC 20 providing a converted error equal to a gain amplifier 22. A gain amplifier 22 provides gain G of the converted error signal from output of the DAC 20 to provide an amplified error signal to the summer 14. The amplified error signal output of the gain amplifier 22 is fed back into the summer 14 to be subtracted from the analog input signal 10 to provide input error signal. Hence, the first order modulator

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comprises a first order feedback loop. The first order feedback loop forces the average of the converted error signal output of the DAC 20 to be equal to the analog input signal 10 plus an error signal. The output of the first order modulator 12 is a series of +1 or -1 pulses of varying duration. The second order modulator of Figure 1B, comprises a first order feedback loop and a second order feedback loop. The second order feedback loop comprises a summer 14a, integrator 16a, a the one bit quantizer 18, a DAC 20a, and a gain amplifier 22a, whereas the first order feedback loop comprises a summer 14b, integrator 16b, the one bit quantizer 18, a DAC 20b, and a gain amplifier 22b. The first order feedback loop serve to generate a first order input error signal at summer 14b, while the second order feedback loop serves to generate a second order input error signal of first order input error signal. The presence of a second order feedback loop reduces the magnitude of the overall error at the binary output 12. The binary output 12 of the sigma delta modulator is a series of pulses of +1 or -1 of varying duration. Hence, the sigma delta modulators convert the analog input 10 into the binary output 12. The sigma delta modulators have been used as modulators for digital communications, and as part of an analog to digital converter. These sigma delta modulators have been used in analog to digital converters comprising a sigma delta modulator and a digital filter. These sigma delta modulators have also been to as opposing modulators and demodulators in communication links for communicating an analog signal by transmitting a binary communication signal through the crosslink. In the sigma delta analog-to-digital converter, the sigma delta modulator and digital interpolating filter are an

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integrated package. While sigma delta modulators offer analog signal modulation, these modulators have not been used for laser crosslink communication where digital signal samples rather than analog samples are desired. These and other disadvantages are solved or reduced using the invention.

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